AMENDMENTS TO THE CLAIMS

Claims 1-11 are pending in this application. Claims 2 and 10 remain as previously pending. Please add new Claims 13-21. Please cancel Claim 12. Please amend Claims 1, 3-9, and 11.

1. (Currently Amended) A method of making a memory module comprising:

attaching at least one memory integrated circuit to a printed circuit board, said printed circuit board comprising data bus contacts on a portion thereof; ~~and~~

coupling said data bus contacts on said printed circuit board to data bus terminals on said memory integrated circuit through a bus switch ~~on said printed circuit board~~; and

interfacing a state decoder with a memory controller, wherein said state decoder selectively controls said bus switch to reduce data bus capacitance.

2. (Original) The method of Claim 1, wherein the memory integrated circuit comprises synchronous DRAM.

3. (Currently Amended) The method of Claim 1, further comprising interfacing ~~a~~the state decoder with the bus switch.

4. (Currently Amended) The method of Claim ~~3~~1, wherein the ~~stated~~ state decoder is structured to decode at least one control gate and control the bus switch in response thereto.

5. (Currently Amended) A method of making a memory module comprising:

attaching at least one memory integrated circuit to a printed circuit board, said printed circuit board comprising data bus contacts on a portion thereof; and

coupling said data bus contacts on said printed circuit board to data bus terminals on said memory integrated circuit; ~~and~~

positioning a bus switch in a data path to the memory integrated circuit; and

interfacing a state decoder with a memory controller, wherein said state decoder selectively controls said bus switch to reduce data bus capacitance.

6. (Currently Amended) The method of Claim ~~1~~5, wherein the memory integrated circuit comprises synchronous DRAM.

7. (Currently Amended) The method of Claim ~~1~~5, ~~additionally~~ further comprising interfacing ~~a~~ the state decoder with the bus switch.

8. (Currently Amended) The method of Claim ~~3~~5, wherein the ~~stated~~ state decoder is structured to decode at least one control gate and control the bus switch in response thereto.

9. (Currently Amended) The method of Claim 5, wherein the memory integrated circuit comprises the bus switch.

10. (Original) The method of Claim 5, wherein the bus switch is positioned externally with respect to the memory integrated circuit.

11. (Currently Amended) A method of making a memory integrated circuit comprising the acts of:

connecting data input terminals to an input portion of a bus switch;

connecting an output portion of said bus switch to a data input buffer; ~~and~~

coupling an output of said data input buffer to a memory storage circuit; and

connecting a state decoder to a memory controller, wherein said state decoder selectively controls said bus switch to reduce data bus capacitance.

12. (Canceled)

13. (New) The method of Claim 1 wherein the bus switch electrically removes a portion of the data bus associated with unaccessed memory circuits.

14. (New) The method of Claim 13 wherein capacitance of unaccessed memory circuits is associated with the portion of the data bus.

15. (New) The method of Claim 1 wherein the memory integrated circuit comprises the bus switch.

16. (New) The method of Claim 1 wherein the memory integrated circuit comprises the state decoder.

17. (New) The method of Claim 5 wherein the memory integrated circuit comprises the state decoder.

18. (New) The method of Claim 11 wherein the state decoder is located within the memory integrated circuit.

19. (New) The method of Claim 11 wherein the bus switch is located within the memory integrated circuit.

20. (New) The method of Claim 11, further comprising interfacing the state decoder with the bus switch.

21. (New) The method of Claim 11, wherein the state decoder is structured to decode at least one control gate and control the bus switch in response thereto.

REMARKS

The December 8, 2004 Office Action was base on pending Claims 1-11 and withdrawn Claim 12. This amendment amends Claims 1, 3-9, and 11, cancels Claim 12, and adds new Claims 13-21. Thus, after entry of the Amendment, Claims 1-11, and 13-21 are pending and presented for further consideration.

In the December 8, 2004 Office Action, the Examiner rejected Claims 1-11. In particular, the Examiner rejected Claims 4 and 10 under 35 U.S.C. § 112, second paragraph. The Examiner further rejected Claims 1, 3, 4, 5, 7, 8, 10, and 11 under 35 U.S.C. § 102(b/e) as being anticipated by U.S. Patent No. 5,303,192 ("the Baba patent") or U.S. Patent No. 6,011,710 ("the Wiggers patent"). The Examiner further rejected Claims 2, 6, and 9 under 35 U.S.C. § 103(a) as being unpatentable over the Baba patent or the Wiggers patent. The Examiner further objected to Claims 6-8 as being substantial duplicates of Claims 2-4.

OBJECTION TO CLAIMS 6-8 UNDER 37 C.F.R. § 1.75

The Examiner objected to Claims 6-8 as being substantial duplicates of Claims 2-4, respectively. Applicant has amended Claims 6-8 to depend from Claim 5. Withdrawal of the objection to Claims 6-8 under 37 C.F.R. § 1.75 is requested.

REJECTION OF CLAIMS 4 AND 10 UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

With respect to Claim 4, the Examiner has stated that the limitation of "the stated decoder" in line 1 has insufficient basis. Applicant has amended "the stated decoder" to "the state decoder" in Claim 4 line 1, which provides sufficient basis.

With respect to Claim 10, the Examiner has stated that the limitation "the bus switch" in line 1 has insufficient basis. Applicant has amended "a switch" in line 6 of Claim 5 to "a bus switch". Amended Claim 5 provides sufficient basis for Claim 10, which depends from Claim 5.

Withdrawal of the rejection of Claims 4 and 10 under 35 U.S.C. § 112, second paragraph is requested.

REJECTION OF CLAIMS 1, 3-5, 7, 8, 10, AND 11 UNDER 35 U.S.C. § 102(b)

The Examiner rejected Claims 1, 3-5, 7, 8, 10, and 11 under 35 U.S.C. § 102(b) as being anticipated by the Baba patent. In view of the following discussion, Applicant respectfully traverses this rejection.

Claims 1, 5, 11

Baba appears to teach a bus line switching circuit selectively connecting N memory elements among M memory elements to N external bus lines. A control circuit appears to detect when the address signal has address information indicative of a defective memory cell and to control the bus switch so that memory elements having defective blocks are not selected. Baba does not teach interfacing a state controller with a memory controller, where the state decoder controls the bus switch to reduce data bus capacitance.

In contrast, in an embodiment of the invention, a method of making a memory module comprises interfacing a state decoder with a memory controller, where the state decoder selectively controls a bus switch to reduce data bus capacitance.

The reference cited by the Examiner does not disclose, teach, or suggest the use of a state decoder where the state decoder selectively controls a bus switch to reduce data bus capacitance. Applicant asserts that Claims 1, 5, and 11 are not anticipated by the Baba patent. Applicant therefore respectfully submits that Claims 1, 5, and 11 are patentably distinguished over the cited reference and Applicant respectfully requests allowance of Claims 1, 5, and 11.

Claims 3, 4, 7, 8, and 10

Claims 3 and 4, which depend from Claim 1, and Claims 7, 8, and 10, which depend from Claim 5, are believed to be patentable for the same reasons articulated above with respect to Claims 1 and 5, respectively, and because of the additional features recited therein.

REJECTION OF CLAIMS 1, 3-5, 7, 8, 10, AND 11 UNDER 35 U.S.C. § 102(e)

The Examiner rejected Claims 1, 3-5, 7, 8, 10, and 11 under 35 U.S.C. § 102(e) as being anticipated by the Wiggers patent. In view of the following discussion, Applicant respectfully traverses this rejection.

Claims 1, 5, 11

Wigger also does not appear to teach interfacing a state controller with a memory controller, where the state decoder controls the bus switch to reduce data bus capacitance.

In contrast, in an embodiment of the invention, a method of making a memory module comprises interfacing a state decoder with a memory controller, where the state decoder selectively controls a bus switch to reduce data bus capacitance.

The reference cited by the Examiner does not disclose, teach, or suggest the use of a state decoder where the state decoder selectively controls a bus switch to reduce data bus capacitance. Applicant asserts that Claims 1, 5, and 11 are not anticipated by the Wiggers patent. Applicant therefore respectfully submits that Claims 1, 5, and 11 are patentably distinguished over the cited reference and Applicant respectfully requests allowance of Claims 1, 5, and 11.

Claims 3, 4, 7, 8, and 10

Claims 3 and 4, which depend from Claim 1, and Claims 7, 8, and 10, which depend from Claim 5, are believed to be patentable for the same reasons articulated above with respect to Claims 1 and 5, respectively, and because of the additional features recited therein.

REJECTION OF CLAIMS 2, 6, AND 9 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 2, 6, and 9 under 35 U.S.C. § 103(a) as being unpatentable over the Baba patent or the Wiggers patent.

Claim 2, which depends from Claim 1, and Claims 6 and 9, which depend from Claim 5, are believed to be patentable for the same reasons articulated above with respect to Claims 1 and 5, respectively, and because of the additional features recited therein.

NEW CLAIMS

New Claims 13-21 have been added to more fully define the Applicant's invention and are believed to be fully distinguished over the prior art of record.

New Claims 13-16 depend from amended Claim 1 and are believed to be allowable for the same reasons articulated above with respect to Claim 1, and because of the additional features recited therein.

New Claim 17 depends from amended Claim 5 and is believed to be allowable for the same reasons articulated above with respect to Claim 5, and because of the additional features recited therein.

New Claims 18-21 depend from amended Claim 11 and are believed to be allowable for the same reasons articulated above with respect to Claim 11, and because of the additional features recited therein.

REQUEST FOR TELEPHONE INTERVIEW

Pursuant to M.P.E.P. § 713.01, in order to expedite prosecution of this application, Applicant's undersigned attorney of record hereby formally requests a telephone interview with the Examiner as soon as the Examiner has considered the effect of the arguments presented above. Applicant's attorney can be reached at (949) 721-2998 or at the number listed below.

CONCLUSION

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. In light of the above remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 3/7/05

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